AMENDMENTS TO THE CLAIMS:

Please cancel without prejudice claims 1 and 15-18 and amend claims 2-4, 6-9, 19, 21

and 22 as follows.

This listing of claims will replace all prior versions, and listings, of claims in the

application:

1. (cancelled).

2. (currently amended) A controller as claimed in Claim ~~1~~6, wherein the data buffer of at

least one of the at least ~~one~~two channel~~s~~ is arranged to store prior to transmission on the data link

data items relating to at least one data element specified by the control data, and the interface

mechanism is arranged to be responsive to the control data to transmit on the data link in the

corresponding at least one data slot, data items retrieved from the data buffer.

3. (currently amended) A controller as claimed in Claim ~~1~~6, wherein the data buffer of at

least one of the at least ~~one~~two channel~~s~~ is arranged to store data items received from the data

link and relating to at least one data element as specified by the control data, and the interface

mechanism is arranged to be responsive to the control data to store, in the data buffer, data items

received from the corresponding at least one data slot.

4. (currently amended) A controller as claimed in Claim ~~1~~6, wherein each channel

comprises a pair of said data buffers and their associated control registers, one of said data

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buffers arranged to store data items to be transmitted on the data link, and the other of said data

buffers arranged to store data items received from the data link.

5. (cancelled)

6. (currently amended) A controller for controlling interfacing to a data link, the data link

enabling data items relating to a number of data elements to be transferred in corresponding data

slots of the data link, the controller comprising:

at least ~~one~~two channels, each channel comprising a data buffer for storing data items,

and a control register associated with the data buffer and arranged to store control data, the

control data settable to identify at least one data element whose corresponding data items are to

be stored in the data buffer; and

an interface mechanism for controlling the transfer of data items between the at least ~~one~~

two channels and the data slots of the data link in dependence upon said control data, wherein

~~each~~the data buffer of each channel is arranged to store data items relating to one or more data

elements having the same sampling rate, where data items relating to data elements having

different sampling rates are stored to respective data buffers of different channels.

7. (currently amended) A controller as claimed in Claim ~~1~~6, wherein the controller is

connectable to a codec via the data link.

8. (currently amended) A controller as claimed in Claim ~~1~~6, wherein each data buffer

comprises a first-in-first-out (FIFO) buffer.

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9. (currently amended) A controller as claimed in Claim ~~16~~, further comprising a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel.

10. (original) A controller as claimed in Claim 9, wherein the memory interface couples the controller to the memory via a processor arranged to control access to the memory.

11. (previously presented) A controller for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data settable to identify at least one data element whose corresponding data items are to be stored in the data buffer;

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data; and

a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel, wherein each control register has a first field settable to indicate a compact mode in which data words passed between the associated data buffer and the memory comprise a plurality of said data items.

12. (original) A controller as claimed in Claim 11, wherein data items are represented as a fixed size when transferred in the data slots, and each control register has a second field settable to indicate the actual size of data items stored in the associated data buffer, and if the first field is set the memory interface is arranged to reference the second field in order to determine how many data items are to be included in each data word passed between the associated data buffer and the memory.

13. (previously presented) A controller for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data settable to identify at least one data element whose corresponding data items are to be stored in the data buffer;

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data; and

a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel,, wherein data items are represented as a fixed size when transferred in the data slots, and each control register has a field settable to indicate the actual size of each data item stored in the associated data buffer, thereby enabling the memory interface to convert the data items between the actual size and the fixed size.

14. (previously presented) A controller for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data settable to identify at least one data element whose corresponding data items are to be stored in the data buffer;

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data; and

a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel,, wherein the control data within the control register specifies the number of data elements whose data items are stored in the associated data buffer, and the memory interface is arranged to control the rate of transfer of data between the data buffer and the memory dependent on the control data.

15. (cancelled).

16. (cancelled).

17. (cancelled).

18. (cancelled).

19. (currently amended) A controller ~~as claimed in Claim 9~~for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data settable to identify at least one data element whose corresponding data items are to be stored in the data buffer;

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data, wherein the number of channels provided by the controller is less than the number of data elements whose data items are capable of being transferred by the data link; and

comprising a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel, wherein each control register has a first field settable to indicate a compact mode in which data words passed between the associated data buffer and the memory comprise a plurality of said data items.

20. (previously presented) A controller as claimed in Claim 11, wherein data items are represented as a fixed size when transferred in the data slots, and each control register has a second field settable to indicate the actual size of data items stored in the associated data buffer, and if the first field is set the memory interface is arranged to reference the second field in order to determine how many data items are to be included in each data word passed between the associated data buffer and the memory.

21. (currently amended) A controller ~~as claimed in Claim 9~~for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data settable to identify at least one data element whose corresponding data items are to be stored in the data buffer;

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data, wherein the number of channels provided by the controller is less than the number of data elements whose data items are capable of being transferred by the data link; and

comprising a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel, wherein data items are represented as a fixed size when transferred in the data slots, and each control register has a field settable to indicate the actual size of each data item stored in the associated data buffer, thereby enabling the memory interface to convert the data items between the actual size and the fixed size.

22. (currently amended) A controller ~~as claimed in Claim 9~~for controlling interfacing to a data link, the data link enabling data items relating to a number of data elements to be transferred in corresponding data slots of the data link, the controller comprising:

at least one channel, each channel comprising a data buffer for storing data items, and a control register associated with the data buffer and arranged to store control data, the control data

settable to identify at least one data element whose corresponding data items are to be stored in the data buffer;

an interface mechanism for controlling the transfer of data items between the at least one channel and the data slots of the data link in dependence upon said control data, wherein the number of channels provided by the controller is less than the number of data elements whose data items are capable of being transferred by the data link; and

comprising a memory interface for coupling the controller to a memory, to enable data items to be transferred between the memory and the at least one channel, wherein the control data within the control register specifies the number of data elements whose data items are stored in the associated data buffer, and the memory interface is arranged to control the rate of transfer of data between the data buffer and the memory dependent on the control data.

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